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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,153	12/10/2003	Donald E. Steiss	22347-08260 (8116)	7373

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EXAMINER	
TREAT, WILLIAM M	
ART UNIT	**PAPER NUMBER**
2181	

MAIL DATE	DELIVERY MODE
08/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,153	STEISS ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-19,21-38,40-53 and 55-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2 and 4-19* is/are allowed.

6)☒ Claim(s) *21-38,40-53 and 55-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/12/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-2, 4-19, 21-38, 40-53, and 55-68 are presented for examination.

2. When finding art for the elected invention, the examiner saw that the art found encompassed the non-elected invention so the examiner has withdrawn the restriction and applied art to the claims, as appropriate.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 21-26, 28, 30, 32, 34, 38, 52, and 66-68 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Rohlman et al. (Publication No. 20010032307).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1-2, 11-18, 26-27, 29, 31, 33, 35-37, 46-51, 53, and 61-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rohlman et al. (Publication No. 20010032307).

8. The reasons, set forth in the examiner's previous action for rejecting claims 21-38, 48-53, and 61-68 over Rohlman, continue and are hereby incorporated by reference.

9. Applicant's arguments filed 6/8/2007 have been fully considered but they are not persuasive.

10. Applicants have argued on behalf of claims 21-38, 46-53, and 61-68: Rohlman does not disclose (a) "an upper pipeline, having an input coupled to receive a signal indicative of an instruction queue depth corresponding to a plurality of threads, the upper pipeline determining an instruction fetch sequence for the plurality of threads based on the instruction queue depth signal; and a lower pipeline, comprising a first input to receive decoded instructions and a second input to receive a thread conditions signal, the lower pipeline determining a thread execution sequence based on the thread conditions signal, the thread conditions signal indicative of an execution stall corresponding to the plurality of threads" and (b) "selecting a thread associated with a high priority instruction from the plurality of threads, selecting a thread associated with a low priority instruction from the plurality of threads, and selecting the thread between the

thread associated with the high priority instruction and the thread associated with the low priority instruction."

11. As to 10(a), there is no universally accepted definition in the art for upper pipeline and lower pipeline. The only universally accepted aspect of upper pipelines and lower pipelines is that the upper pipeline precedes the lower pipeline. Note, in paragraph [0055] to which applicants were referred, Rohlman states: "As described above, the trace cache 410 and the micro-instruction sequencer 420 may have a counter that keeps track of the number of micro-ops stored in the micro-op queue 432. In multi-thread mode, this counter can also be useful for the trace cache 410 and the micro-instruction sequencer 420 to determine on which thread the units should issue micro-ops. A counter may be provided for each thread, and when the memory locations of one of the threads becomes full or approaches full the trace cache 410 or the micro-instruction sequencer 420 can issue micro-ops on the other thread. For example, if a counter monitoring T0 indicates that the T0 memory locations 451-460 are full, the trace cache 410 will issue micro-ops from its T1 portion 412." The examiner views the trace cache and microinstruction sequencer as being components of the upper pipeline of Rohlman. Inherently, the trace cache 410 and the micro-instruction sequencer 420 must be receiving a signal/signals indicative of an instruction queue depth from the micro-op queue 432 or some other component of the lower pipeline or the trace cache 410 and the micro-instruction sequencer 420 could not track whether the T0 or T1 memory locations in the micro-op queue were becoming full. Also, in paragraph [0054] to which applicants were referred, Rohlman states: "The micro-instruction queue 430

can also be used to limit the number of stalls when the processor is operating in multi-thread mode. As described above, when a stall occurs on one thread, the micro-instruction queue 430 can switch to another thread. However, even though this may save some pipe stages, there still may be some micro-ops that are lost on the thread having the stall condition. Thus, a decrease in the number of stalls results in fewer lost micro-ops. The micro-instruction queue 430 may be used to monitor the pipeline resources on the threads and compare these resources. The micro-instruction queue 430 may then select the thread having more available resources, decreasing the probability of a stall. For example, through a feedback loop, the micro-instruction queue 430 can monitor the resources available in the execution unit 440. For example, there may be more available space in the T0 portion 441 of execution unit 440 than in the T1 portion 442 of execution unit 440. In this case, the micro-instruction queue 430 can select T0 because there are more available resources on that thread. Thus, the number of stalls can be limited and the bandwidth of the processor can be improved." Whether the signals received by the microinstruction queue are indicative of an actual stall or a potential stall (both conditions discussed by Rohlman, above), the micro-op queue (i.e., the lower pipeline) receives thread condition signals indicative of an execution stall. Note too, that the micro-op queue receives decoded instructions (i.e., in Fig. 4 there is no decoder for the micro-ops which follows the micro-op queue).

12. As to 10(b), Rohlman, inherently, assigns a dynamic execution priority to his plurality of threads (T0, T1). The executing thread has a higher priority than the idle thread (i.e., the executing thread has the higher execution priority and the idle thread

has the lower execution priority). As conditions in the pipeline evolve, as when a stall condition develops (see paragraph [0054], Rohlman's system stops selecting the executing (high-execution-priority) thread and selects the idle (low-execution-priority) thread. At the same time, the newly executing thread dynamically becomes the high-execution priority thread and the newly idle thread becomes the low-execution-priority thread.

13. Claims 34-38, 40-43, 45, 52-53, 55-58, 60 and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemirovsky et al. (Publication No. 20020062435).

14. Claims 35-38, 40-51, 53, and 55-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky et al. (Publication No. 20020062435).

15. The reasons, set forth in the examiner's previous action for rejecting claims 34-38, 40-53, 55-65, and 68 over Nemirovsky, continue and are hereby incorporated by reference.

16. Applicants have argued on behalf of claims 34-38, 40-53, 55-65, and 68: Nemirovsky does not disclose "selecting a thread associated with a high priority instruction from the plurality of threads, selecting a thread associated with a low priority instruction from the plurality of threads, and selecting the thread between the thread associated with the high priority instruction and the thread associated with the low priority instruction." In paragraph [0061] Nemirovsky taught: "In embodiments of the invention priority control unit 9 determines the context wherein priorities are interpreted by instruction scheduler 5 to allocate instructions. For example, the stream with the highest priority may always take precedence over a stream with a lower priority.

Alternatively, the scheduler may guarantee minimal access to all streams, but increase access in proportion to a stream's priority." This is what applicants have asserted distinguishes their claims from Nemirovsky.

17. Claims 1-2 and 4-19 are allowable over the prior art of record.

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

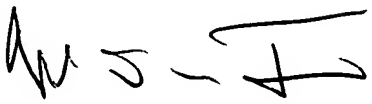
19. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

William M. Treat



Primary Examiner